**PATENT** 

Docket No.: 60188-448

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Keiichi FUJIMOTO, et al.

Confirmation Number: 2785

Serial No.: 09/964,480V

Group Art Unit: 2829

/Serial 110.. 05/50 1, 100 -

Allowed: December 02, 2003

Filed: September 28, 2001

Examiner: Patel

For: SEMICONDUCTOR INTEGRATED CIRCUIT TESTING SYSTEM AND

**METHOD** 

## REQUEST FOR ACKNOWLEDGEMENT OF THE CITED ART

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

We are in receipt of the Notice of Allowance dated December 02, 2003.

In reviewing the file, it is noted that we have not received acknowledgement of the Information Disclosure Statement and cited art filed November 12, 2003. Enclosed are copies of the Information Disclosure Statement, PTO-1449 and stamped return postcard acknowledgement.

Applicants hereby respectfully requests that:

the appropriately acknowledged PTO-1449 be furnished to Applicants; and the record be clarified to confirm that the cited art has been considered and made of record.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Mogarty Registration No. 36,139

600 13<sup>th</sup> Street, N.W. Washington, DC 20005-3096 (202) 756-8000 MEF:blp Facsimile: (202) 756-8087 Date: January 9, 2004

WDC99 860753-1.060188.0448

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**METHOD** 

## **LETTER SUBMITTING FORMAL DRAWINGS**

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In response to the Notice of Allowability dated December 02, 2003, submitted herewith are nine (09) sheets of Formal Drawings in connection with the above referenced application.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty Registration No. 36,139

600 13<sup>th</sup> Street, N.W. Washington, DC 20005-3096 (202) 756-8000 MEF:blp Facsimile: (202) 756-8087

Date: January g 3004

	Applic	cant:	) Keiichi FUJIMOTO, et al.						<u> </u>	Docket No					00/004 400				
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